3/IDS 2825
E. Shillinger
10-29-03

ESMC-01-450

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To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/042,074 01/08/02

Dun-Nian Yaung et al.

GRID METAL DESIGN FOR LARGE DENSITY CMOS IMAGE SENSOR

Grp. Art Unit: 2825

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on February 27, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B. Ackerman 2/27/02

U.S. Patent 5,278,105 to Eden et al., "Semiconductor Device with Dummy Features in Active Layers," discloses a method in which dummy features are introduced to increase the percentage of material remaining after etch and thereby to reduce the loading affect.

U.S. Patent 5,798,298 to Yang et al., "Method of Automatically Generating Dummy Metals for Multilevel Interconnection," discloses using dummy metal shaped in blocks to prevent the loading affect during etching for multilevel interconnection.

U.S. Patent 5,915,201 to Chang et al., "Trench Surrounded Metal Pattern," discusses dummy metal areas with sizes similar to the functional metal lines distributed among the functional lines reducing the loading affect.

U.S. Patent 5,926,733 to Heo, "Metal Layer Patterns of a Semiconductor Device and a Method for Forming the Same," discusses using dummy metal patterns to reduce loading affects.

U.S. Patent 6,180,448 to Lee, "Semiconductor Memory Device Having a Capacitor Over Bitline Structure and Method for Manufacturing the Same," discusses using dummy storage electrodes to alleviate the loading affect.

Sincerely,

Stephen B Ackerman

Stephen B. Ackerman, Reg. #37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-01-450	10/042,074
Applicant	
Dun-Nian Yaung et al.	
Filing Date	**Group Art Unit**
01/08/02	2825

OIPE JC22 MAR 07 2002 PATENT & TRADEMARK OFFICE

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5278105	1/11/94	Eden et al.	437	250	8/19/92
	5798298	8/25/98	Yang et al.	438	622	2/9/96
	5915201	6/22/99	Chang et al.	438	631	10/30/97
	5926733	7/20/99	Heo	438	622	4/2/97
	6180448	1/30/01	Lee	438	253	9/17/98

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.